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EXAMINER	
MOLL, JESSE R	

ART UNIT	PAPER NUMBER
2181	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/056,532	RUSH ET AL.	
	Examiner	Art Unit	
	Jesse R. Moll	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 October 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-39 have been examined.

Acknowledgment of papers filed: amendment filed on 10 October 2006. The papers filed have been placed on record.

Withdrawn Objections / Rejections

2. Applicant, via amendment, has overcome the objections to Claims 11 and 12. The objections are respectfully withdrawn.

3. s

Applicant, via amendment, has overcome the rejections of Claims 4, 19-23 and 25-32. The rejection is respectfully withdrawn.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1, 3-7, 19-24, 26-31, 33-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 (U.S. Patent No. 6,148,354) in view of knowledge common in the art.

6. Regarding claim 1, Ban-354 discloses an apparatus comprising: a receiver (Components 66-76; see fig. 6) to receive bytes of a data packet (write packet; see fig. 9); the receiver to transmit relevant bytes (see col. 7, lines 54-62) of the data packet and to identify irrelevant bytes of the data packet while receiving the bytes of the data packet (Checksum);

Note that the checksum and PID values are not needed by the flash device and are not sent. Error correction is handled by the data handler 76.

And a data customer (MTD 78; see fig. 6) to receive only the relevant bytes of the data packet (see col. 8, lines 12-28).

The term "relevant bytes" can be reasonably interpreted as any data that is received. Any data that is actually received can be considered to be relevant to something. The claim does not contain any limitations that impose a relationship between said "relevant bytes" and said "irrelevant bytes".

Ban-354 does not expressly disclose the receiver is operable to remove the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet.

It was commonly known in the art at the time of the invention to remove the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet.

Since the error correction is done before the data is transferred to the flash components, it is not necessary to send the checksum (needed for error correction) information to the flash components. It was commonly known in the art to remove unnecessary (irrelevant) data before transmitting it.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Ban-354 by removing the identified irrelevant bytes of the data packet prior to transmitting the relevant bytes of the data packet, as commonly known in the art, in order to increase performance and decreasing power consumption by decreasing the amount of data transferred to the flash components.

7. Regarding claim 3, Ban-354 discloses the irrelevant bytes are error correction code bytes (see above regarding claim 1).

8. Regarding claim 4, Ban-354 discloses the receiver is operable to identify the irrelevant bytes upon a receipt of an end of the data packet indication.

Note that it is impossible to identify the CRC value before the end of the packet since packet length is variable (see Applicant's specification, paragraph 0006).

Inherently, the checksum value must be identified after the receipt of the end of data packet indication.

9. Regarding claim 5, Ban-354 discloses the irrelevant bytes are located at an end of the data packet (see fig. 9).

10. Regarding claim 6, Ban-354 discloses the receiver comprises a circuit to identify the irrelevant bytes (Since the bytes are identified, there must be hardware to do this.).

11. Regarding claim 7, Ban-354 discloses the receiver comprises the circuit to delay transmitting of the bytes of the data packet by a predetermined number of bytes (Inherently, the bytes must be delayed or the CRC value would be written to the memory controller.).

12. Claim 19 recites equivalent limitations as claim 1, but is claimed as a method. Claim 19 is rejected as the method the apparatus of claim 1 uses.

13. Regarding claim 20, Ban-354 discloses the receiving the bytes of the data packet is performed via an input bus (USB bus connected to connector 52; see fig. 6).

14. Regarding claim 21, Ban-354 discloses the transmitting the relevant bytes of the data packet comprises utilizing an output bus (Connection to MTD; see fig. 6).

15. Regarding claim 22, Ban-354 discloses the transmitting the relevant bytes of the data packet further comprises transmitting the relevant bytes to a data customer via an output bus (MTD 78).

16. Regarding claim 23, Ban-354 discloses the transmitting the relevant bytes to the data customer comprises informing the data customer that the transmitted bytes are relevant.

Note that in order for MTD 78 to receive data, it must be informed that there is data (such as a clock to latch data).

17. Regarding claim 24, Ban-354 discloses the informing the data customer is performed by asserting an output signal line.

Note that the data customer is informed; therefore there must be at least one signal line to send the information.

18. Claims 26, 27, 28, 29 and 30 recite equivalent limitations as claims 3, 4, 7, 13 and 6 and are rejected under the same grounds.

19. Regarding claim 31, Ban-354 discloses the circuit comprises a plurality of storage elements (USB buffer; see col. 2, lines 41-53).

20. Claim 33 recites equivalent limitations as claim 19 and is rejected under the same grounds.

21. Claim 34 recites equivalent limitations as claim 20 and is rejected under the same grounds.

22. Claim 35 recites equivalent limitations as claim 7 and is rejected under the same grounds.

23. Claim 37 recites equivalent limitations as claim 4 and is rejected under the same grounds.

24. Claim 38 recites equivalent limitations as claim 23 and is rejected under the same grounds.

25. Claim 39 recites equivalent limitations as claim 24 and is rejected under the same grounds.

26. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 in view of Miklos (U.S. Patent No. 6,621,796 B1).

27. Ban-354 discloses a circuit comprising: a plurality of storage elements (USB buffer; see col. 2, lines 41-53) to delay transmitting of bytes of a data packet by a predetermined number of bytes (see above regarding claim 7); and a third input signal to indicate an end of the data packet and to cancel advancement through the plurality of storage elements of bytes stored in the plurality of storage elements,

Note that there must be a signal to determine the end of a packet otherwise the device would never know when to send the data to the flash device.

Ban-354 does not expressly disclose a first input signal to indicate presence of a valid byte of the data packet on an input data bus; a second input signal to advance the byte through the plurality of storage elements; and the third input signal combined with the second input signal to indicate presence of an irrelevant byte on an output data bus.

Miklos teaches a first input signal to indicate presence of a valid byte of the data packet on an input data bus (see col. 18, lines 46-67); a second input signal to advance the byte through the plurality of storage elements (multiple bytes in a buffer require a pointer to the current item; the items must be accessible sequentially and a signal is used to advance through them); and the third input signal combined with the second input signal to indicate presence of an irrelevant byte on an output data bus.

Note that when the end of the packet is received, the next byte would be irrelevant to that packet. That byte would be on the output bus when it goes through the buffer.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354 by adding a first input signal to

indicate presence of a valid byte of the data packet on an input data bus; a second input signal to advance the byte through the plurality of storage elements; and the third input signal combined with the second input signal to indicate presence of an irrelevant byte on an output data bus, as taught by Miklos, in order to decrease memory in the sender and receiver (see Miklos, col. 18, line 62-67).

28. Claims 10, 17 and 18 rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 in view of Miklos further in view of Ban-168 (U.S. Patent No. 5,799,168).

29. Regarding claim 10, Ban-354/Miklos disclose the circuit of claim 9 further comprising: a first output signal to indicate presence of a relevant byte of the data packet on the output data bus (latch signal for the Data register; see Ban-168; col. 3, lines 35-37);

Note that for data to be sent to the flash device, data must be sent to the data register. This device must be signaled that there is data available in the data register. This signal is the first output signal

And a second output signal to indicate the end of the data packet (data for the Count register; see Ban-168; col. 4, lines 14-15).

Note that the end of the packet is indicated by how many writes are to be done. Further note that Ban-354 discloses that the flash controller of Ban-176 can be used (see col. 8, lines 25-28). Therefore it would have been obvious for one of ordinary skill

in the art to have modified used the flash controller of Ban-176 in the invention of Ban-354.

30. Regarding claim 17, Ban-354/Ban-168/Miklos disclose the circuit of claim 10 wherein an asserted second input signal and an asserted third input signal de-assert the first output signal (see above regarding claims 9 and 10).

Note that asserting signals or de-asserting signals makes no functional difference in the invention.

31. Regarding claim 18, Ban-354/Ban-168/Miklos discloses the circuit of claim 17 wherein the de-asserted first output signal indicates a presence of an irrelevant byte on the output data bus (see above regarding claim 10).

32. Claims 11 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 in view of Miklos and Ban-168 further in view of Patchen (U.S. Patent No. 4,970,407).

33. Regarding claims 11 and 12, Ban-354/Ban-168/Miklos disclose the circuit of claim 10.

Ban-354 does not expressly disclose each storage element is a flip flop or a latch.

Patchen teaches each storage element is a flip flop and a latch (see abstract).

Note that the device taught by Patchen is both a flip flop and a latch.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354/Ban-168/Miklos by using flip flops and latches as storage elements, as taught by Patchen, in order to efficiently and flexibly load and store data (see Patchen, col. 1, lines 25-34).

34. Claims 2, 8, 25, 32 and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 in view of knowledge common in the art.

35. Regarding claim 2, Ban-354 discloses the apparatus of claim 1.

36. Ban-354 does not expressly disclose the receiver to transmit the relevant bytes of the data packet prior to a receipt of an end of the data packet indication.

37. Examiner asserts that it was commonly known in the art to start transferring data before receiving the entire packet.

38. It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354 by transmitting the relevant bytes of the data packet prior to a receipt of an end of the data packet indication, as commonly known in the art, in order to decrease latency and to decrease buffer size. Since USB packets can be 1024 bytes long, it is unreasonable to build the invention of Ban-354 with a 1024 bit wide bus between the USB buffer and the Flash controller.

39. Regarding claim 8, Ban-354 discloses the apparatus of claim 7.

Ban-354 does not expressly disclose the predetermined number of bytes equals to a number of the irrelevant bytes.

Examiner asserts that it was commonly known in the art to only delay a transmission by a minimum value.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354 by making the predetermined number of bytes equal to a number of the irrelevant bytes, as commonly known in the art, in order to decrease latency and improve performance.

40. Claim 25 recites equivalent limitations as claim 2 and is rejected under the same grounds.

41. Regarding claim 32, Ban-354 discloses the apparatus of claim 31.

Ban-354 does not expressly disclose a total number of the plurality of the storage elements is equal to ((the number of irrelevant bytes+1) times a width of an input bus)+((the number of the irrelevant bytes+1) times 2)).

Examiner asserts that it was commonly known in the art to use large buffers to decrease the impact of in consistent data rates. Commonly used buffers for USB were 64 bytes. With an 8-bit bus, the claim limits the number of storage elements to 40. In a 64-byte buffer, the last 40 bits can be considered to be said storage elements.

It would have been obvious at the time of the invention for one of ordinary skill in the art to have modified the invention of Ban-354 by using a total number of the plurality of the storage elements equal to ((the number of irrelevant bytes+1) times a width of an input bus)+((the number of the irrelevant bytes+1) times 2)), as commonly known in the art, in order to decrease the effect of inconsistent data transfers and increase data throughput.

42. Regarding claim 36, Ban-354 discloses the apparatus of claim 35.

Ban-354 does not expressly disclose the predetermined number of bytes equals to a one greater than a number of the irrelevant bytes.

Examiner asserts that it was commonly known in the art to read a byte and perform a check on that byte in a later clock cycle.

As combined above regarding claim 8, the delay is equal to the number of irrelevant bytes. However, if a byte were checked to determine if it is the last byte one clock cycle after it is read, the minimum delay would be the number of irrelevant bytes plus one.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354 by making the predetermined number of bytes equals to a one greater than a number of the irrelevant bytes, as commonly known in the art, in order to decrease clock cycle time and increase performance by decreasing stage complexity.

43. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ban-354 in view of Miklos and Ban-168 in further view of knowledge common in the art.

44. Claim 13 recites equivalent limitations as claim 36 and is rejected using the same reasons.

45. Regarding claims 14 and 16, Ban-354/Ban-168/Miklos discloses the circuit of claim 10.

Ban-354/Ban-168/Miklos does not expressly disclose the second input signal and the third input signal control the first output signal by controlling output signals of a plurality of multiplexers to control the plurality of storage elements.

Examiner asserts that it was commonly known in the art to use multiplexers to control the output and signals of a buffer.

It would have been obvious for one of ordinary skill in the art at the time of the invention to have modified the invention of Ban-354/Ban-168/Miklos by making the second input signal and the third input signal control the first output signal by controlling output signals of a plurality of multiplexers to control the plurality of storage elements, as known commonly in the art, in order to make design easier because multiplexer designs of buffers are commonly known.

46. Claim 15 recites equivalent limitations as claim 32 and is rejected using the same reasons.

Response to Arguments

47. Applicant's arguments with respect to claims 1 and 3-7, 19-32 and 33-39 have been considered but are moot in view of the new ground(s) of rejection.

48. Applicant's arguments with respect to claims 9-18 have been fully considered but they are not persuasive.

As stated in the previous action, the device as disclosed by Ban-354 (or the combination with Miklos) ***must*** contain a signal to indicate an end of the data packet and to cancel advancement through the plurality of storage elements. In order to correctly write or read to the flash components, something must indicate the end of the packet. Additionally, the indication of the end of the packet must force the device to stop sending information to the flash device. If the signal does not do these two operations, reading and writing to the flash components would not be possible.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP

§ 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

49. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse R. Moll whose telephone number is (571)272-2703. The examiner can normally be reached on M-F 10:00 am - 6:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Fritz M. Fleming can be reached on 571-272-4145. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Jesse R Moll
Examiner
Art Unit 2181

JM 6/27/06

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SUPERVISORY PATENT EXAMINER